EMBEDDED PROCESSOR WITH DUAL-PORT SRAM FOR PROGRAMMABLE LOGIC

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for programmable logic devices including embedded processors having a dual-port SRAMs. A programmable logic integrated circuit includes a programmable logic portion having a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions, and an embedded processor portion coupled to the programmable logic portion. The embedded processor portion includes a processor, and a memory block coupled to the processor. The memory block includes a first plurality of memory cells for storing data, a second plurality of memory cells for storing data, a first port coupled to the first and second pluralities of memory cells, a second port coupled to the first and second pluralities of memory cells, and an arbiter coupled to the first port and the second port. When the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.